A Fully-Integrated Low-Power Low-Noise 2.6-GHz Bipolar VCO for Wireless Applications

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***Abstract*—The low quality factor of the inductors fabricated in fully-integrated LC tanks results in a poor indirect stability of the oscillators, which are therefore highly sensitive to low-frequency noise and disturbances coupled through substrate and supply lines. The paper addresses the design of a 2-V voltage-controlled oscillator (VCO) at 2.6 GHz fabricated in a Si-bipolar process with f_T of 20 GHz. The circuit bias and the transistor layout have been specifically optimized to minimize the phase noise degradation due to the intrinsic low indirect stability. A single sideband-to-carrier ratio (SSCR) of -104 dBc/Hz at 100 kHz is demonstrated with less than 14 mW power consumption.**

***Index Terms*—Bipolar transistor oscillators, oscillator stability, phase noise, voltage controlled oscillators.**

I. Introduction

THE high phase noise level in the voltage-controlled oscillator (VCO) embedded in the frequency synthesizer, is one of the major limitations to the full integration of transceivers for wireless applications. For this reason many demonstrations of low phase noise integrated oscillator have recently appeared in literature. The rush toward even better performance has however hidden a conceptual aspect so far: the low Q-factor of the fully-integrated LC tanks intrinsically leads to poor indirect stability of these circuits.

In practice, the VCO frequency f_0 is not simply set by the tank, but also by the additional loop phase delay θ due to the active elements. From basic oscillator theory f_0 may be written as [1]

$$f_0 = \frac{1}{2\pi\sqrt{LC}}\left(1 - \frac{\theta}{2Q}\right). \tag{1}$$

The delay θdepends on the transistor bias current. Therefore its low-frequency noise, as well as the disturbances from substrate and from supply lines, can modulatef_0, leading to phase noise degradation [2]. For this reason the good noise performance achieved in a stand-alone VCO can be highly degraded once it is embedded into a complete transceiver.

This paper presents a fully-integrated VCO at 2.6 GHz specifically designed to minimize the impact of the weak indirect stability on phase noise performance. Those are often expressed in terms of single sideband-to-carrier ratio (SSCR), the ratio between the noise power S_V at an offset f_0 from the carrier and

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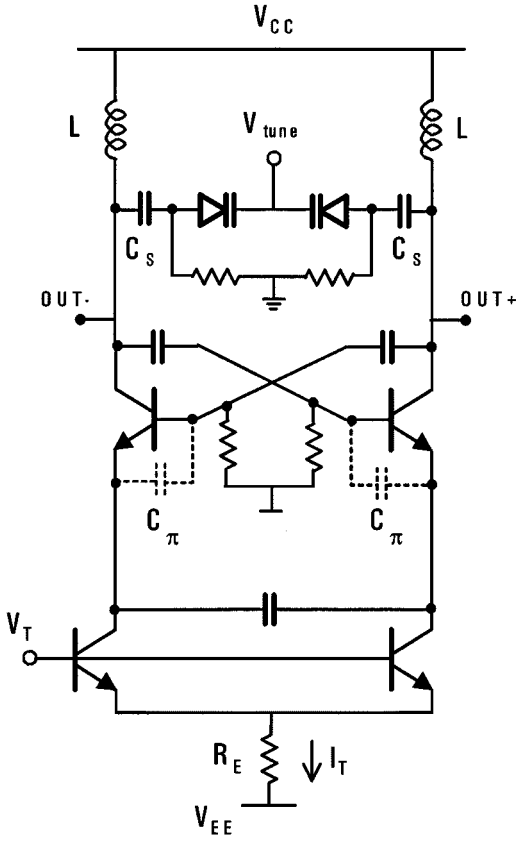

Fig. 1. Differential oscillator schematic.

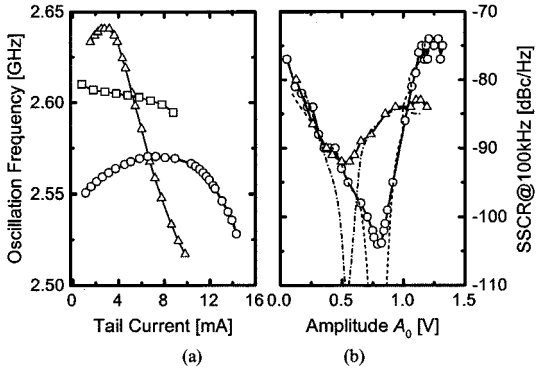

Fig. 2. (a) Measurements of oscillation frequency versus tail current for a nonoptimized (triangles) and for the optimized oscillator (dots); simulated behavior of a 0.35 μm-complementary metal oxide semiconductor (CMOS) oscillator with similar circuit topology (squares). (b) Measured and estimated *SSCR@*100 kHz for the nonoptimized (solid line with triangles, and dash-dotted line, respectively) and for the optimized VCO (solid line with dots, and dashed line).

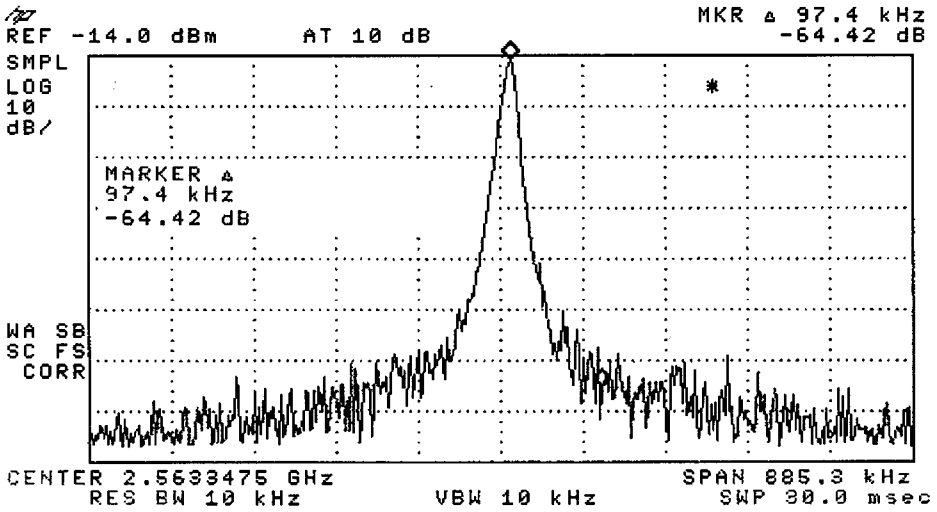

Fig. 3. Spectrum analyzer snapshot of the optimal SSCR@100 kHz for the optimized oscillator.

the power of the carrier itself $A_0^2/2$. The circuit has been implemented in a bipolar technology with n-p-n devices having a maximum f_T of 20 GHz [3] and spiral inductors with a quality factor Q of about 8. The design has been optimized for low power consumption.

II. Oscillator Optimization

Fig. 1 shows the circuit topology. The oscillator's indirect stability was quoted by measuring f_0 versus the bias current, I_T; the triangles in Fig. 2(a) were obtained from a first implementation of the circuit, with 3-V power supply. The shape of the curve can be easily interpreted, referring to (1). In that formula the phase shift θ is due to the transistors' base transit time ($\tau_T \approx C_\pi/g_m$) which depends on the bias current:

1) at low I_T, the main contribution to the stray capacitance C_π is the junction capacitance, which is almost constant with bias current. Therefore the transit time decreases as I_T grows and the oscillation frequency increases;
2) at high currents, C_π increases steeply due to the base push-out effect [4], thus reducing the oscillation frequency.

The sensitivity $|\partial f_0/\partial I_T|$ the low-frequency noise of I_T, having a power spectral density S_{I_T}, and the output *SSCR* at f_n from the carrier. The noise of I_T modulates the output frequency, therefore it results, [2]

$$SSCR(f_n) = \frac{1}{2}\left(\frac{\partial f_0}{\partial I_T}\right)^2 \frac{S_{I_T}(f_n)df}{f_n^2}. \tag{2}$$

This effect explains the measured *SSCR* dependence on the oscillation amplitude A_0 [solid line with triangles—Fig. 2(b)]. In fact A_0 can be increased only by rising I_T, thus changing the sensitivity of the circuit itself to the bias current noise and substrate disturbances. The SSCR reaches a minimum when $|\partial f_0/\partial I_T|$ is zero, then it rises again. The dash-dotted line in Fig. 2(b) was computed by measuring S_{I_T} and then plugging it into (2).

Better performance could therefore be achieved by smoothing the f_0 dependence on I_T and shifting the frequency peak (where the sensitivity is zero) to a larger I_T. For this purpose the layout of the transistor pair was changed. While in the first circuit the devices featured a square emitter area of 18 μm^2, in a second version the emitter area was enlarged to 72 μm^2 and drawn interdigitated in the layout, thus displacing the onset of high injection effects to larger I_T.

The changes prove quite effective. The circles in Fig. 2(a) show the dependence of f_0 vs. I_T for the new circuit. The f_0 peak has been shifted up from 3 to 6.5 mA, and the maximal derivative $|\partial f_0/\partial I_T|$ has been reduced from 25 down to 3.5 MHz/mA. The minimum *SSCR* [circles in Fig. 2(b)] displaces to a nearly doubled A_0, as expected, and improves from -92 to -104 dBc/Hz. Such a reduction is larger than the 6 dB expected, because also the $r_{bb'}$ thermal noise of the differential pair decreases.

Since the new circuit is less sensitive to tail current noise, the resistance R_E was removed, making it possible the reduction of the power supply from 3 V to 2 V. The power consumption is now less than 14 mW. Fig. 3 shows the output spectrum of the optimized oscillator. At 2-V supply the VCO tuning range is 250 MHz, or about 10% of the center frequency.

III. Comparison with the Prior Art

Fig. 4 sketches the comparison of the VCO performance with the ones reported in literature, both in bipolar and CMOS technologies [9]–[16]. Since the *SSCR* depends on both the term $(f_0/f_n)^2$ and on A_0, i.e., on the oscillator power consumption, an appropriate figure of merit (*FOM*) is

$$FOM = \left(\frac{f_0}{f_n}\right)^2 \frac{1}{P \cdot SSCR(f_n)} \tag{3}$$

where P is the power dissipation of the oscillator, expressed in milliwatts [5]. Note that the delivered output power instead is not directly related to the *SSCR* performance. The VCO presented in this work ranks as the best among the bipolar ones,

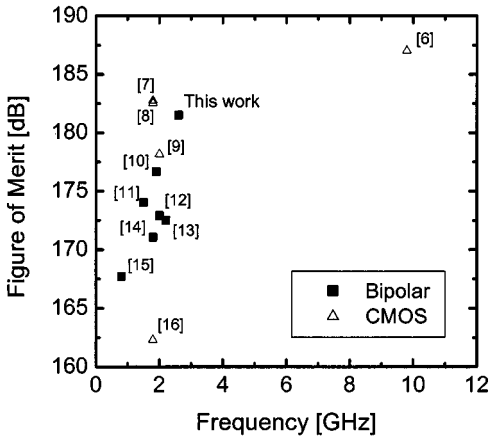

Fig. 4. *FOM* computed on recently reported VCOs' using spiral inductors.

the improvements is mainly to the understanding and elimination of the main phase noise mechanism. The circuit in [6] capitalizes on its quite high oscillation frequency to attain a figure better than the one of the novel oscillator; indeed, [7] and [8] also are close. In all of these cases the VCOs' were CMOS-built. CMOS VCOs' usually outperform their bipolar counterpart, even featuring higher flicker noise, because their sensitivity to the tail current disturbances is practically zeroed. The squares in Fig. 2(a) outline the f_0 dependence as simulated for a CMOS VCO designed with the same topology as in Fig. 1, using a $0.35\ \mu$m technology. It is apparent that the bipolar VCOs' design is much more critical for what concerns the isolation from low-frequency noise and disturbances. However, in this work we have demonstrated how it can be judiciously handled and optimized.

IV. Conclusion

A fully-integrated 2.6-GHz voltage-controlled oscillator (VCO) with low phase noise and low power consumption has been fabricated in a 20-GHz Si-bipolar process. The low noise performance has been obtained by minimizing the impact of low-frequency noise and disturbances coming from the tail. At this aim the transistors of the differential pair have been designed to move their peak of f_{T} at high currents. The new design allows for the adoption of a lower supply voltage with a corresponding decrease of the power consumption.

References

[1] K. K. Clarke and D. T. Hess, *Communication Circuits: Analysis and Design*. Reading, MA: Addison-Wesley, 1971.

[2] C. Samori, A. L. Lacaita, A. Zanchi, S. Levantino, and G. Cali, "Phase noise degradation at high oscillation amplitudes in LC-tank VCOs," *IEEE J. Solid-State Circuits*, vol. 35, pp. 96–99, Jan. 2000.

[3] G. Cali, G. Cantone, P. Filoramo, G. Sirna, P. Vita, and G. Palmisano, "A high-performance Si-Bipolar RF receiver for digital satellite radio," *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 2568–2576, Dec. 1998.

[4] P. A. H. Hart, *Bipolar and Bipolar-MOS Integration*. Amsterdam, The Netherlands: North-Holland, 1994.

[5] J. Plouchart, H. Ainspan, M. Soyuer, and A. Ruehli, "A fully monolithic SiGe differential VCO for 5 GHz wireless applications," in *Proc.2000 IEEE RFIC Symp.*, Boston, MA, June 2000, pp. 5–60.

[6] H. Wang, "A 9.8 GHz back-gate tuned VCO in $0.35\ \mu$m CMOS," in *Proc. Dig. Tech. Papers, ISSCC '99*, San Francisco, CA, pp. 406–407.

[7] J. Craninckx and M. Steyaert, "A 1.8-GHz Low Phase Noise VCO Using Optimized Hollow Spiral Inductors," *IEEE J. Solid-State Circuits*, vol. 32, pp. 736–744, May 1997.

[8] A. Hajimiri and T. Lee, "Design Issues in CMOS differential LC oscillators," *IEEE J. Solid-State Circuits*, vol. 34, pp. 717–724, May 1999.

[9] B. De Muer, C. De Ranter, and M. Steyaert, "A fully integrated 2 GHz LC-VCO with phase noise of -125 dBc/Hz at 600 kHz," in *Proc. ESSCIRC '99*, Duisburg, Germany, Sep. 1999, pp. 206–209.

[10] T. Wakimoto and S. Konaka, "A 1.9-GHz Si Bipolar Quadrature VCO with Fully-Integrated LC Tank," in *Proc. 1998 Symp. VLSI Circuits*, Honolulu, HI, Jun. 11–13, 1998, pp. 30–31.

[11] L. Dauphinee, M. Copeland, and P. Schvan, "A balanced 1.5 GHz voltage controlled oscillator with an integrated LC resonator," in *Proc. Dig. Tech. Papers, ISSCC '97*, San Francisco, CA, pp. 390–391.

[12] M. Zannoth, B. Kolb, J. Fenk, and R. Weigel, "A fully integrated VCO at 2 GHz," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1987–1991, Dec. 1998.

[13] B. Jansen, K. Negus, and D. Lee, "Silicon bipolar VCO family from 1.1 to 2.2 GHz with fully-integrated tank and tuning circuits," in *Proc. Dig. Tech. Papers, ISSCC '97*, San Francisco, CA, pp. 392–393.

[14] A. Wagemans, P. Baltus, R. Dekker, A. Hoogstraate, H. Maas, A. Tombeur, and J. van Sinderen, "A 3.5 mW 2.5 GHz diversity receiver and a 1.2 mW 3.6 GHz VCO in silicon-on-anything," in *Proc. Dig. Tech. Papers, ISSCC '98*, San Francisco, CA, pp. 250–251.

[15] M. A. Margarit, J. L. Tham, R. G. Meyer, and M. J. Deen, "A low-noise, low-power VCO with automatic amplitude control for wireless applications," *IEEE J. Solid-State Circuits*, vol. 34, pp. 761–771, Jun. 1999.

[16] C. Lam and B. Razavi, "A 2.6 GHz/5.2 GHz CMOS voltage-controlled oscillator," in *Proc. Dig. Tech. Papers, ISSCC '99*, San Francisco, CA, pp. 402–403.